instruction for determining a class of each function and for causing the instruction to be executed by those said elements which perform those associated said logical sequences affecting the instruction execution in an optimum manner[, said element selection logic means portion for causing the instruction to be executed by those said elements which perform those associated said logical sequences affecting the instruction execution in an optimum manner includes means for transmitting and switching signals to said elements optically].

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11. (Twice Amended) In a computer including a memory for holding a sequence of instructions to be executed, logic for accessing the instructions in sequence, logic for determining for each instruction a function to be performed and an effective address thereof, and logic for executing each instruction, a method of operation <u>by said computer, wherein said logic for executing each instruction comprises a plurality of individual elements on a common support substrate with each element optimized to perform certain logical sequences employed in executing instructions, said method</u> comprising <u>for each instruction</u> the steps of:

[a) providing a plurality of individual elements on a common support substrate with each element optimized to perform certain logical sequences employed in executing instructions; and for each instruction,]

[b)] <u>a)</u> determining the function to be performed;

[c)] <u>b)</u> determining a class of each function;

[d)] <u>c)</u> causing the instruction to be executed by those elements which perform the associated logical sequences affecting the instruction execution in an optimum manner [by optically transmitting and switching signals to the elements].

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19. (Twice Amended) A computer comprising:

a) a memory for holding a sequence of instructions to be executed;

b) logic for accessing said instructions in sequence;

c) logic for determining for each said instruction a function to be performed and an effective address thereof;

d) a plurality of individual elements on a common support substrate optimized to perform certain logical sequences employed in executing said instructions; and,

e) element selection logic means connected to said logic determining the function to be performed for each said instruction for determining a class of each function and for causing the instruction to be executed by those said elements which perform those associated said logical sequences affecting the instruction execution in an optimum manner[, said element selection logic means portion for causing the instruction to be executed by those said elements which perform those associated said logical sequences affecting the instruction execution in an optimum manner including means for transmitting and switching signals to said elements optically].

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37. (Once Amended) In a computer including a memory for holding a sequence of instructions to be executed, logic for accessing the instructions in sequence, logic for determining for each instruction a function to be performed and an effective address thereof, and logic for executing each instruction, the improvement wherein:

a) the logic for executing instructions comprises:

a plurality of individual elements on a common support substrate optimized to perform certain logical sequences employed in executing instructions; and [additionally comprising,]

b) the computer comprises:

element selection logic means connected to the logic determining the function to be performed for each instruction for determining a class of each function and for causing the instruction to be executed by those said elements which perform those associated said logical sequences affecting the instruction execution in an optimum manner, said element selection logic means including means for accepting dynamic inputs designating changes in an operating environment of the computer and means for changing the ones of said elements which execute each instruction as a function of said dynamic inputs whereby instruction execution is affected in an optimum manner for the present dynamic conditions.

Please add the following new claims, which reinstate previously cancelled claims 5, 13 and 23, respectively:

--39. (New) The improvement to a computer of claim 1 wherein:

said element selection logic means portion for causing the instruction to be executed by those said elements which perform those associated said logical sequences affecting the instruction execution in an optimum manner includes means for transmitting and switching signals to said elements optically.--

--40. (New) The method of claim 11 wherein said step of causing the instruction to be executed by the elements which perform those associated logical sequences affecting the instruction execution in an optimum manner includes the step of:

optically transmitting and switching signals to the elements.--

--41. (New) The computer of claim 19 wherein: